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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al.

Title: ULTRA HIGH DENSITY FLASH MEMORY

Docket No.: 303.330US3

Serial No.: 09/866,938

Filed: May 29, 2001

Due Date: N/A

Examiner: Jack Chen

Group Art Unit: 2813

Commissioner for Patents
Washington, D.C. 20231

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We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ A Supplemental Information Disclosure Statement (1 pg.), Form 1449 (6 pgs.), and copies of 120 cited references.
- ☒ A Communication Concerning Co-Pending Applications (3 pgs.).

Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: *Raymond R. Berdie*
Atty: Raymond R. Berdie
Reg. No. 50,769

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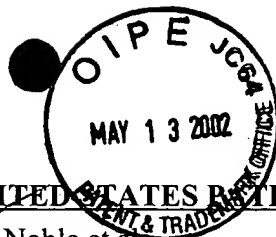
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S/N 09/866,938



PATENT

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WENDELL P. NOBLE ET AL.

By their Representatives,

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By

Raymond R. Berdie

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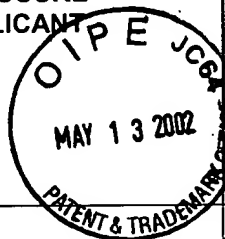
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Application Number	09/866938
Filing Date	May 29, 2001
First Named Inventor	Noble Jr., Wendell
Group Art Unit	2813
Examiner Name	Chen, Jack

Sheet 1 of 6

Attorney Docket No: 00303.330US3

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
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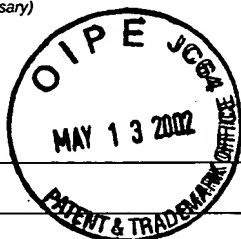
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Examiner Name	Chen, Jack

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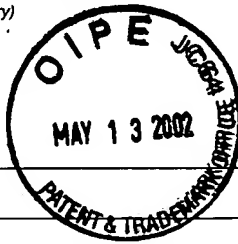
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Sheet 4 of 6

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Substitute Disclosure Statement Form (PTO-1449)

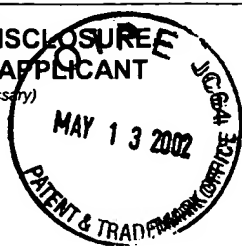
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	09/866938
Filing Date	May 29, 2001
First Named Inventor	Noble Jr., Wendell
Group Art Unit	2813
Examiner Name	Chen, Jack

Sheet 6 of 6

Attorney Docket No: 00303.330US3

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Amsterdam, (1994), pp. 601-663	
		SZE, S.M., VLSI Technology, 2nd Edition, Mc Graw-Hill, NY, (1988), 90	
		TAKATO, H., et al., "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSIs", IEEE International Electron Devices Meeting, Technical Digest, (1988), 222-225	
		TEMLER, D., "Multilayer Vertical Stacked Capacitors (MVSTC) for 64Mbit and 256Mbit DRAMs", 1991 Symposium on VLSI Technology, Digest of Technical Papers, Oiso, (May 28-30, 1991), 13-14	
		VITTAL, A., et al., "Clock Skew Optimization for Ground Bounce Control", 1996 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, San Jose, CA, (Nov. 10-14, 1996), 395-399	
		WANG, P.W., et al., "Excellent Emission Characteristics of Tunneling Oxides Formed Using Ultrathin Silicon Films for Flash Memory Devices", Japanese Journal of Applied Physics, 35, (June 1996), 3369-3373	
		WATANABE, H., et al., "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", 1993 Symposium on VLSI Technology, Digest of Technical Papers, Kyoto, Japan, (1993), 17-18	
		WATANABE, H., et al., "An Advanced Fabrication Technology of Hemispherical Grained (HSG) Poly-Si for High Capacitance Storage Electrodes", Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, Japan, (1991), 478-480	
		WATANABE, H., et al., "Device Application and Structure Observation for Hemispherical-Grained Si", J. Appl. Phys., 71, (Apr. 1992), 3538-3543	
		WATANABE, H., et al., "Hemispherical Grained Silicon (HSG-Si) Formation on In-Situ Phosphorous Doped Amorphous-Si Using the Seeding Method", Extended Abstracts of the 1992 International Conference on Solid State Devices and Materials, Tsukuba, Japan, (1992), 422-424	
		YOSHIKAWA, K., "Impact of Cell Threshold Voltage Distribution in the Array of Flash Memories on Scaled and Multilevel Flash Cell Design", 1996 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu, HI, (June 11-13, 1996), 240-241	

EXAMINER**DATE CONSIDERED**

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